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INTERNATIONAL TELECOMMUNICATION UNION

CCITT **V.17**

THE INTERNATIONAL
TELEGRAPH AND TELEPHONE
CONSULTATIVE COMMITTEE

DATA COMMUNICATION
OVER THE TELEPHONE NETWORK

A 2-WIRE MODEM FOR FACSIMILE APPLICATIONS WITH RATES UP TO 14 400 bit/s

Recommendation V.17

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FOREWORD

permanent organ of the International Telecommunication Union (ITU). CCITT is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The Plenary Assembly of CCITT which meets every four years, establishes the topics for study and approves Recommendations prepared by its Study Groups. The approval of Recommendations by the members of CCITT between Plenary Assemblies is covered by the procedure laid down in CCITT Resolution No. 2 (Melbourne, 1988).

Recommendation V.17 was prepared by Study Group XVII and was approved under the Resolution No. 2 procedure on the 22 of February 1991.

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CCITT NOTE

indicate both a telecommunication Administration and a recognized private operating agency.

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A 2 -WIRE MODEM FOR FACSIMILE APPLICATIONS WITH
RATES UP TO 14 400 bit/s

1 Introduction

This Recommendation defines the modulation methods and operating sequences for a modem intended only for use in high speed facsimile applications.

Appropriate T-Series Recommendations should be consulted regarding operating procedures and other features employed in facsimile transmission applications, as these differ from those recommended for high speed modems for general applications.

The modem has the following principal characteristics:

a) Provision for half duplex operation at data signalling rates of:
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b) Quadrature amplitude modulation with synchronous line transmission at 2400 symbols per second.

c) Inclusion of data scramblers, adaptive equalizers and eight-state trellis coding.

d) Two sequences for training and synchronization: long train and resync.

2 Line signals

2.1 *Carrier frequency*

The channel carrier frequency is 1800 ± 1 Hz. The receiver must be able to operate with received frequency offsets of up to ± 7 Hz.

2.2 *Modulation*

The modulation rate shall be 2400 ± 0.01% symbols per second.

2.3 *Signal element codings*

2.3.1 *Signal element codings for 14 400 bit/s*

The scrambled data stream to be transmitted is divided into groups of six consecutive data bits, which are ordered according to their time of occurrence. As shown in Figure 1/V.17, the first two bits in each group, Q1n and Q2n (where n designates the sequence number of the group) are first differentially encoded into Y1n and Y2n according to Table 1/V.17.

Figure 1/V.17 = 13.5 cm

µTABLE 1/V.17

Differential coding for use with trellis coding

Input

Previous outputs

Outputs

Q1n

Q2n

Y1n—1

Y2n—1

Y1n

Y2n

0
0
0
0

0
0
0
0

1
1
1
1

1
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1
1

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The two differentially encoded bits Y1n and Y2n are used as inputs to a systematic convolutional encoder which generates a redundant bit Y0n. This redundant bit and the six information-carrying bits Y1n, Y2n, Q3n, Q4n, Q5n and Q6n are then mapped into the coordinates of the signal element to be transmitted according to the signal space diagram shown in Figure 2/V.17.

Figure 2/V.17 = 21 cm

2.3.2 *Signal element codings for 12 000 bit/s*

The scrambled data stream to be transmitted is divided into groups of five consecutive data bits, which are ordered according to their time of occurrence. As shown in Figure 1/V.17, the first two bits in each group, Q1n and Q2n (where n designates the sequence number of the group) are first differentially encoded into Y1n and Y2n according to Table 1/V.17.

The two differentially encoded bits Y1n and Y2n are used as inputs to a systematic convolutional encoder which generates a redundant bit Y0n. This redundant bit and the five information-carrying bits Y1n, Y2n, Q3n, Q4n and Q5n are then mapped into the coordinates of the signal element to be transmitted according to the signal space diagram shown in Figure 3/V.17.

Figure 3/V.17 = 18.5 cm

2.3.3 *Signal element codings for 9600 bit/s*

The scrambled data stream to be transmitted is divided into groups of four consecutive data bits, which are ordered according to their time of occurrence. As shown in Figure 1/V.17, the first two bits in each group, Q1n and Q2n (where n designates the sequence number of the group) are first differentially encoded into Y1n and Y2n according to Table 1/V.17.

The two differentially encoded bits Y1n and Y2n are used as inputs to a systematic convolutional encoder which generates a redundant bit Y0n. This redundant bit and the four information-carrying bits Y1n, Y2n, Q3n and Q4n are then mapped into the coordinates of the signal element to be transmitted, according to the signal space diagram shown in Figure 4/V.17.

Figure 4/V.17 = 13 cm

2.3.4 *Signal element codings for 7200 bit/s*

The scrambled data stream to be transmitted is divided into groups of three consecutive data bits, which are ordered according to their time of occurrence. As shown in Figure 1/V.17, the first two bits in each group, Q1n and Q2n (where n designates the sequence number of the group) are first differentially encoded into Y1n and Y2n according to Table 1/V.17.

The two differentially encoded bits Y1n and Y2n are used as inputs to a systematic convolutional encoder which generates a redundant bit Y0n. This redundant bit and the three information-carrying bits Y1n, Y2n and Q3n are then mapped into the coordinates of the signal element to be transmitted according to the signal space diagram shown in Figure 5/V.17.

Figure 5/V.17 = 11 cm

2.4 *Transmitted spectra*

With continuous binary ONEs applied to the input of the scrambler, the transmitted energy density at 600 Hz and 3000 Hz should be attenuated by 4.5 ± 2.5 dB with respect to the maximum energy density between 600 Hz and 3000 Hz.

3 Interchange circuits

3.1 *List of interchange circuits*

References in the Recommendation to V.24 interchange circuit numbers are intended to refer to the functional equivalent of such circuits and are not intended to imply the physical implementation of such circuits. For example, references to circuit 103 should be understood to refer to the functional equivalent of circuit 103 (see Table 2/V.17).

µTABLE 2/V.17

Interchange circuits

Number	Description
102	Signal ground or common return
103	Transmitted data
104	Received data
105	Request to send
106	Ready for sending
107	Data set ready
108/1 or	Connect data set to line (Note)
108/2	Data terminal ready (Note)
109	Data channel received line signal detector
114	Transmitter signal element timing (DCE source)
115	Receiver signal element timing (DCE source)
125	Calling indicator

Note — This circuit shall be capable of operating as circuit 108/1 or circuit 108/2.

3.2 *Transmit data*

The modem shall accept data from the facsimile control function on circuit 103; the data on circuit 103 shall be under the control of circuit 114.

3.3 *Receive data*

The modem shall pass data to the facsimile control function on circuit 104; data on circuit 104 shall be under the control of circuit 115.

3.4 *Timing arrangements*

Clocks shall be included in the modem to provide the facsimile control function with transmitter element timing on circuit 114 and receiver signal element timing on circuit 115.

3.5 *Data rate control*

This shall be provided by a connection between the modem and the facsimile control function; the nature of this connection is beyond the scope of this Recommendation.

3.6 *Circuits 106 and 109 response times*

After the training and synchronizing sequences defined in § 5, circuit 106 shall follow OFF to ON or ON to OFF transitions of circuit 105 within 3.5 ms. The OFF to ON transition of circuit 109 is part of the training sequence specified in § 5. Circuit 109 shall turn OFF 30 to 50 ms after the level of the received signal appearing at the line terminal of the modem falls below the relevant threshold defined in § 3.7. Following a dropout, after the initial handshake, circuit 109 shall turn ON 40 to 205 ms after the level of the received signal appearing at the line terminal of the modem exceeds the relevant threshold defined in § 3.7.

3.7 *Circuit 109 threshold*

> —43 dBm ON.

> —48 dBm OFF.

The condition of circuit 109 between the ON and OFF levels is not specified except that the signal detector shall exhibit a hysteresis action, such that the level at which the OFF to ON transition occurs shall be at least 2 dB greater than that for the ON to OFF transition.

Circuit 109 thresholds are specified at the input to the modem when receiving scrambled binary ONEs.

Administrations are permitted to change these thresholds where transmission conditions are known.

Note — Circuit 109 ON to OFF response time should be suitably chosen within the specified limits to ensure that all valid data bits have appeared on circuit 104.

3.8 *Clamping*

The DCE shall hold, where implemented, circuit 104 in the binary ONE condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition and, where required to protect circuit 104 from false signals, for a period of 150 ± 25 ms following the ON to OFF transition on circuit 105. The use of this additional delay is optional, based on system considerations.

4 Scrambler and descrambler

The modem shall use a self-synchronizing scrambler/descrambler with the generator polynomial:

At the transmitter, the scrambler shall effectively divide the message data sequence by the generating polynomial. The coefficients of the quotient of this division, taken in descending order, form the data sequence which shall appear at the output of the scrambler. At the receiver, the received data sequence shall be multiplied by the scrambler generating polynomial to recover the message sequence.

5 Operating sequences

5.1 *Training and synchronizing sequences*

Two separate sequences of training and synchronizing signals are defined in Table 3/V.17.

The long train sequence is for initial establishment of a connection or for retraining when needed.

The resync. sequence is for resynchronization after a successful long train.

µTABLE 3/V.17

Training and synchronizing signals

	Segment 1	Segment 2	Segment 3	Segment 4		
	ABAB alternations	Equalizer training signal	Bridge signal	Scrambled ONEs	Total symbol interval	Approximate time (ms)
Long train	256	2976	64	48	3344	1393
Resync.	256	~~2938~~	64	48	~~3342~~	~~1142~~

5.1.1 *Segment 1: ABAB alternations*

This segment consists of alternations between states A and B as shown in Figures 2/V.17 to 5/V.17.

5.1.2 *Segment 2: equalizer training signal*

This segment consists of the sequential transmission of four signal elements A, B, C, and D as shown in Figures 2/V.17 to 5/V.17.

The equalizer conditioning pattern is a pseudo-random sequence at 4800 bit/s generated by the $1 + x^{-18} + x^{-23}$ data scrambler. During segment 2, any differential quadrant encoding is disabled and the scrambled dibits are encoded as shown in Table 4/V.17.

With a binary ONE applied to the input, the initial scrambler state shall be selected to produce the following scrambler output pattern and corresponding signal elements:

µTABLE 4/V.17

Encoding for four phase training signal

Segment 2

Dibit	Signal state
00	C
01	D
00	C
01	D
00	C
01	D
00	C
01	D
00	C
01	D
00	C
01	D
10	B
01	D
10	B
01	D

5.1.3 *Segment 3: bridge signal*

This segment, which is used only during an initial long train, consists of a 16-bit binary sequence transmitted eight times. The sequence as defined in Table 5/V.17 is scrambled, and transmitted at 4800 bit/s using the signal elements A, B, C, and D as defined in Figures 2/V.17 to 5/V.17.

µTABLE 5/V.17

Segment 3: Bit designations

B

B

B

B

B

B

B

B

B

B

B

B

B

B

B

B

0

1

2

3

4

5

6

7

8

The dibits are differentially encoded as defined in Table 6/V.17.

The differential encoder shall be initialized using the final symbol of the previous segment. The first two bits and subsequent dibits of each 16-bit sequence shall be encoded as one signal state.

µTABLE 6/V.17

Segment 3: Dibit encoding

Dibit	Phase change	Previous output/output
00	+ 90 degrees	A/B, B/C, C/D, D/A
01	0 degrees	A/A, B/B, C/C, D/D
10	180 degrees	A/C, B/D, C/A, D/B
11	— 90 degrees	A/D, B/A, C/B, D/C

5.1.4 *Segment 4*

Scrambled binary ONEs shall be sent at the channel data bit rate.

For the long train sequence, the differential encoder shall be initialized using the first symbol of segment 3.

For the short train sequence, the differential encoder shall be initialized using the last symbol of segment 2.

The convolutional encoder initial state shall be initialized to zero.

The scrambler shall be clocked at the bit rate and the scrambler output sequence encoded as defined in § 4. The initial scrambler state is that state produced by the last symbol interval of the previous segment.

The duration of segment 4 is 48 symbol intervals. At the end of segment 4, circuit 106 is turned ON and data are applied to the input of the data scrambler.

Circuit 109 shall be turned ON during the reception of segment 4.

5.2 *Turn OFF sequence*

After an ON to OFF transition of circuit 105, the line signals emitted after remaining data or the end of the training check signal during retrain procedure have been transmitted are shown in Table 7/V.17.

µTABLE 7/V.17

Turn OFF sequence

Segment A	Segment B	Total of segments	Approximate time
Continuous scrambled ONEs	No transmitted energy		
32 SI	48 SI	80 SI	33 ms

SI denotes Symbol intervals

Note — If an OFF to ON transition of circuit 105 occurs during the turn OFF sequence, it will not be taken into account until the end of the turn OFF sequence.

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5.3 *Talker echo protection (TEP) signal*

A TEP signal may, optionally, be transmitted prior to the transmission of training and synchronization sequences. The TEP signal shall consist of an unmodulated carrier for a duration of 185 to 200 ms followed by a silent period of 20 to 25 ms.

When used, the TEP signal shall be considered as part of the training sequences.

Alternative methods for achieving the intended benefits of a TEP signal are for further study.